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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,296	08/26/2003	Masahiro Kimura	59795 (47793)	5390

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EXAMINER	
KNAPP, JUSTIN R	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/649,296	KIMURA ET AL.	
	Examiner	Art Unit	
	Justin Knapp	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2003 and 15 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/26/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Application/Control Number: 10/649,296
Art Unit: 2182

Examiner Notes

1. The PTO-1449 form was not received with the IDS filed 03/24/05. Please re-submit the form.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 2 and 3 are rejected under 35 U.S.C. 112, 2nd paragraph. The claims recite the limitation "said main memory". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 6, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (herein AAPA) in view of Tanenbaum, Structured Computer Organization 3rd Ed.

6. As per claims 1 and 8, AAPA teaches:

two independent buses which are a system bus and a local bus (page 3, section [0007] of Specification);

a main memory coupled to said system bus, capable of transferring data (page 3, section [0007] of Specification);

a local memory coupled to said local bus, capable of transferring data (page 3, section [0007] of Specification); and

AAPA does not explicitly teach a decode unit comprising a decode circuit coupled between said system bus and said local bus, capable of transferring data mutually and developing liquid ejection data compressed to be developed in line based on hardware. AAPA does teach that compressed liquid ejection data is conventionally developed by a program based on software (page 5, section [0015]). Tanenbaum teaches that hardware and software are logically equivalent (page 11). Any operation performed by software can also be built directly into the hardware and any instruction executed by the hardware can also be simulated in software. Using the teaching's of Tanenbaum, it would have been obvious to one of ordinary skill in the art at the time the invention was made to perform the same operation in software taught by AAPA and perform that same operation using hardware. One would have been motivated to do so as the operation is performed frequently enough to justify constructing hardware circuitry to execute them directly making them faster (Tanenbaum, page 11).

7. As per claim 6, AAPA teaches wherein said compressed liquid ejection data is run length compressed data, and said decode circuit is capable of developing run length compressed data based on hardware (page 2, section [0003]).

8. Claims 2-5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (herein AAPA) in view of Tanenbaum in further view Kodota et al (Kodota), US Pub No 2001/0043723 A1

9. As per claim 2, AAPA in view of Tanenbaum teaches:

two independent buses which are a system bus and a local bus (page 3, section [0007] of Specification);

a local memory coupled to said local bus, capable of transferring data (page 3, section [0007] of Specification).

AAPA in view of a Tanenbaum teaches a decode circuit coupled between said system bus and said local bus, capable of transferring data mutually and developing liquid ejection data compressed to be developed in line based on hardware (as taught in the rejection of claims 1 and 8;)

Neither AAPA nor Tanenbaum teach a line buffer for storing liquid ejection data developed by said decode circuit per word unit; and a DMA-transferring means for DMBA-transferring liquid ejection data compressed to be developed in line from said main memory to said decode circuit, DMA-transferring liquid ejection data developed in said line buffer to said local memory per word unit and DMA-transferring developed liquid ejection data stored in said local memory to be a register of an liquid ejection head sequentially. Due to a lack of antecedent basis for a "said main memory", the best reasonable interpretation is given. Kodota teaches a line buffer and a DMA controller for storing and transferring image data in a printer for an encoding circuit (figure 2A, elements 48 and 49, sections [0072] through [0075]). It would have been obvious to one of ordinary skill in the art to utilize the line buffer and DMA transferring

teachings of Kodota in the decoding taught by AAPA in view of Tanenbaum. One would have been motivated to do so as it solves a similar problem, storing encoded/decoded image data and transferring it to be printed via DMA transferring thus eliminating the need for CPU intervention.

10. As per claim 3, AAPA in view of Tanenbaum in further view of Kodota does not explicitly teach wherein registers of said main memory, said decode unit and said liquid ejection head are incorporated in an ASIC as a circuit block, and registers of said decode unit and said liquid ejection head are coupled through an exclusive bus in said ASIC. Official Notice is taken that that use of ASIC circuitry is notoriously well known in the art as it provides a design with a specific application in mind and thus it is optimized for that application from the viewpoint of performance.

11. As per claim 4, AAPA in view of Tanenbaum in further view of Kodota teaches wherein said line buffer comprising two sides of buffer areas capable of storing developed data of predetermined words, liquid ejection data developed by said decode circuit is sequentially stored in one of said sides and liquid ejection data developed by said decode circuit is sequentially stored in the other of said sides when developed data of predetermined words has been accumulated, while developed data of predetermined words is DMA-transferred to said local memory for each predetermined words when developed data of predetermined words has been accumulated. AAPA in view of Tanenbaum in further view of Kodota provides all the necessary components to be capable of such functionality.

12. As per claim 5, AAPA in view of Tanenbaum in further view of Kodota does not explicitly teach wherein data transfers with respect to said local bus from said decode circuit to

said local memory and from said local memory to a register of said liquid ejection head are performed in a burst transfer. Official notice is taken that the use of burst transfers in the DMA art is notoriously well known thus it would have been obvious to one of ordinary skill in the art to utilize DMA burst transfers as it saves on the overhead of setting up a transfer for each data unit.

13. As per claim 7, Kodota teaches wherein said decode unit comprises a means for storing uncompressed liquid ejection data DMA-transferred from said main memory without developing by said decode circuit based on hardware (figure 2a, element 46).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin Knapp whose telephone number is (571)272-4149. The examiner can normally be reached on Mon - Fri 8:30 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dov Popovici can be reached on (571)272-4083. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Justin Knapp
Examiner
Art Unit 2182

June 16, 2005